WE CLAIM:

1. A digital filter of a DPLL (Digital Phase locked loop) comprising:

a first reloadable register portion for storing a TBW (total bandwidth) value, wherein said first reloadable register portion is capable of being coupled to a first port for inputting said TBW value that is programmed into said first reloadable register portion through said first port;

a second reloadable register portion for storing a DBW (differential bandwidth) value, wherein said second reloadable register portion is capable of being coupled to a second port for inputting said DBW value that is programmed into said second reloadable register portion through said second port;

an up_counter for generating an UP_CNT value by counting up each UP signal pulse generated by a phase transition detector when a first phase of a SDIN (serial data input) signal leads a second phase of a current ACLK (recovered clock) signal generated by a phase selector;

a down_counter for generating a DOWN_CNT value by counting up each DOWN signal pulse generated by said phase transition detector when said first phase of said SDIN (serial data input) signal lags said second phase of said current ACLK (recovered clock) signal;

an adder for adding said UP_CNT value and said DOWN_CNT value to generate a SUM value;

a subtractor for generating a DELTA value that is the difference between said UP_CNT value and said DOWN_CNT value;

a delta comparator for asserting a LTP (larger than positive) signal if the magnitude of said DELTA value is greater than said DBW value and if said DOWN_CNT value is greater than said UP_CNT value, and for asserting a STN (small than negative) signal if the magnitude of said DELTA value is greater than said DBW value and if said UP_CNT value is greater than said DOWN_CNT value;

a sum comparator for asserting a WE (write enable) signal when said SUM value is greater than said TBW value; and

a phase select controller for asserting a FWD (forward) signal if said LTP signal is asserted when said WE signal is asserted or for asserting a BWD (backward) signal if said STN signal is asserted when said WE signal is asserted;

wherein said phase selector selects another clock signal having a leading phase from said current ACLK signal as a new ACLK (recovered clock) signal when said FWD signal is asserted;

and wherein said phase selector selects another clock signal having a lagging phase from said current ACLK signal as said new ACLK (recovered clock) signal when said BWD signal is asserted;

and wherein said phase selector selects said current ACLK signal to remain as said new ACLK (recovered clock) signal if said FWD signal and said BWD signal are not asserted when said WE signal is asserted.

2. The digital filter of claim 1, further comprising:

a count reset unit for asserting a CTRS (count reset) signal when said WE signal is asserted or when a manual RST (reset) signal is asserted;

wherein said UP_CNT value of said up_counter and said DOWN_CNT value of said down_counter are reset to zero when said CTRS signal is asserted.

3. The digital filter of claim 1, further comprising:

a lock detector for asserting a LOCK signal if said FWD signal and said BWD signal are not asserted for a predetermined number of cycles of said WE signal being asserted.

4. The digital filter of claim 3, further comprising:

a first LK (lock) reloadable register portion for storing a LKTBW (lock total bandwidth) value, wherein said first LK reloadable register portion is capable of being coupled to a first LK port for inputting said LKTBW value that is programmed into said first LK reloadable register portion through said first LK port;

a second LK (lock) reloadable register portion for storing a LKDBW (lock differential bandwidth) value, wherein said second LK reloadable register portion is capable of being coupled to a second LK port for inputting said LKDBW value that is programmed into said second LK reloadable register portion through said second LK port;

a first TK (track) reloadable register portion for storing a TKTBW (track total bandwidth) value, wherein said first TK reloadable register portion is capable of being coupled to a first TK port for inputting said TKTBW value that is programmed into said first TK reloadable register portion through said first TK port;

a second TK (track) reloadable register portion for storing a TKDBW (track differential bandwidth) value, wherein said second TK reloadable register portion is capable of being coupled to a second TK port for inputting said TKDBW value that is programmed into said second TK reloadable register portion through said second TK port;

a first multiplexer for setting said TBW value to said LKTBW value when said LOCK signal is not asserted and for setting said TBW value to said TKTBW value when said LOCK signal is asserted; and

a second multiplexer for setting said DBW value to said LKDBW value when said LOCK signal is not asserted and for setting said DBW value to said TKDBW value when said LOCK signal is asserted.

5. The digital filter of claim 4, wherein a computer system is used for programming said LKTBW value, said LKDBW value, said TKTBW value, and said

TKDBW value into said first LK reloadable register portion, said second LK reloadable register portion, said first TK reloadable register portion, and said second TK reloadable register portion, respectively, by software from said computer system.

6. The digital filter of claim 1, wherein a computer system is used for programming said TBW value and said DBW value into said first reloadable register portion and said second reloadable register portion, respectively, by software from said computer system.

7. The digital filter of claim 1, wherein said phase transition detector, said digital filter, and said phase selector comprise said DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

8. A digital filter of a DPLL (Digital Phase locked loop) comprising:

means for storing a TBW (total bandwidth) value programmed through a first port;

means for storing a DBW (differential bandwidth) value programmed through a second port;

wherein a phase transition detector generates an UP signal pulse when a first phase of a SDIN (serial data input) signal leads a second phase of a current ACLK (recovered clock) signal generated by a phase selector;

and wherein said phase transition detector generates a DOWN signal pulse when said first phase of said SDIN (serial data input) signal lags said second phase of said current ACLK (recovered clock) signal;

means for asserting a FWD signal if a total number of said UP and DOWN signal pulses is at least said TBW value and if the number of said DOWN signal pulses is more than the number of said UP signal pulses by said DBW value;

means for asserting a BWD signal if the total number of said UP and DOWN signal pulses is at least said TBW value and if the number of said UP signal pulses is more than the number of said DOWN signal pulses by said DBW value;

wherein said phase selector selects another clock signal having a leading phase from said current ACLK signal as a new ACLK (recovered clock) signal when said FWD signal is asserted;

and wherein said phase selector selects another clock signal having a lagging phase from said current ACLK signal as said new ACLK (recovered clock) signal when said BWD signal is asserted;

and wherein said phase selector selects said current ACLK signal to remain as said new ACLK (recovered clock) signal if said FWD signal and said BWD signal are not asserted when said total number of said UP and DOWN signal pulses is at least said TBW value.

9. The digital filter of claim 8, further comprising:

means for resetting any count of the UP signal pulses or the DOWN signal pulses to zero when said total number of said UP and DOWN signal pulses is at least said TBW value.

10. The digital filter of claim 8, further comprising:

means for asserting a LOCK signal if said FWD signal and said BWD signal are not asserted for a predetermined time period.

11. The digital filter of claim 10, further comprising:

means for storing a LKTBW (lock total bandwidth) value programmed through a first LK port;

means for storing a LKDBW (lock differential bandwidth) value programmed

through a second LK port;

means for storing a TKTBW (track total bandwidth) value programmed through a first TK port;

means for storing a TKDBW (track differential bandwidth) value programmed through said second TK port;

means for setting said TBW value to said LKTBW value when said LOCK signal is not asserted and for setting said TBW value to said TKTBW value when said LOCK signal is asserted; and

means for setting said DBW value to said LKDBW value when said LOCK signal is not asserted and for setting said DBW value to said TKDBW value when said LOCK signal is asserted.

12. The digital filter of claim 11, further comprising:

means for programming said LKTBW value, said LKDBW value, said TKTBW value, and said TKDBW value into said first LK reloadable register portion, said second LK reloadable register portion, said first TK reloadable register portion, and said second TK reloadable register portion, respectively.

13. The digital filter of claim 8, further comprising:

means for programming said TBW value and said DBW value into said first reloadable register portion and said second reloadable register portion, respectively.

14. The digital filter of claim 8, wherein said phase transition detector, said digital filter, and said phase selector comprise said DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

15. A method for digitally filtering signals generated within a DPLL (Digital

Phase locked loop) comprising:

programming a TBW (total bandwidth) value into a first reloadable register portion disposed within said DPLL and coupled to a first port for inputting said TBW value that is programmed into said first reloadable register portion through said first port;

programming a DBW (differential bandwidth) value within a second reloadable register portion disposed within said DPLL and coupled to a second port for inputting said DBW value that is programmed into said second reloadable register portion through said second port;

generating an UP_CNT value by counting up each UP signal pulse generated by a phase transition detector when a first phase of a SDIN (serial data input) signal leads a second phase of a current ACLK (recovered clock) signal generated by a phase selector;

generating a DOWN_CNT value by counting up each DOWN signal pulse generated by said phase transition detector when said first phase of said SDIN (serial data input) signal lags said second phase of said current ACLK (recovered clock) signal;

adding said UP_CNT value and said DOWN_CNT value to generate a SUM value;

generating a DELTA value that is the difference between said UP_CNT value and said DOWN_CNT value;

asserting a LTP (larger than positive) signal if the magnitude of said DELTA value is greater than said DBW value and if said DOWN_CNT value is greater than said UP_CNT value, and asserting a STN (small than negative) signal if the magnitude of said DELTA value is greater than said DBW value and if said UP_CNT value is greater than said DOWN_CNT value;

asserting a WE (write enable) signal when said SUM value is greater than said

TBW value; and

asserting a FWD (forward) signal if said LTP signal is asserted when said WE signal is asserted, and asserting a BWD (backward) signal if said STN signal is asserted when said WE signal is asserted;

wherein said phase selector selects another clock signal having a leading phase from said current ACLK signal as a new ACLK (recovered clock) signal when said FWD signal is asserted;

and wherein said phase selector selects another clock signal having a lagging phase from said current ACLK signal as said new ACLK (recovered clock) signal when said BWD signal is asserted;

and wherein said phase selector selects said current ACLK signal to remain as said new ACLK (recovered clock) signal if said FWD signal and said BWD signal are not asserted when said WE signal is asserted.

16. The method of claim 15, further comprising:

asserting a CTRS (count reset) signal when said WE signal is asserted or when a manual RST (reset) signal is asserted; and

resetting said UP_CNT value of said up_counter and said DOWN_CNT value of said down_counter to zero when said CTRS signal is asserted.

17. The method of claim 15, further comprising:

asserting a LOCK signal if said FWD signal and said BWD signal are not asserted for a predetermined number of cycles of said WE signal being asserted.

18. The method of claim 17, further comprising:

programming a LKTBW (lock total bandwidth) value into a first LK (lock) reloadable register portion coupled to a first LK port for inputting said LKTBW value

that is programmed into said first LK reloadable register portion through said first LK port;

programming a LKDBW (lock differential bandwidth) value into a second LK (lock) reloadable register portion coupled to a second LK port for inputting said LKDBW value that is programmed into said second LK reloadable register portion through said second LK port;

programming a TKTBW (track total bandwidth) value into a first TK (track) reloadable register portion coupled to a first TK port for inputting said TKTBW value that is programmed into said first TK reloadable register portion through said first TK port;

programming a TKDBW (track differential bandwidth) value into a second TK (track) reloadable register portion coupled to a second TK port for inputting said TKDBW value that is programmed into said second TK reloadable register portion through said second TK port;

setting said TBW value to said LKTBW value when said LOCK signal is not asserted, and setting said TBW value to said TKTBW value when said LOCK signal is asserted; and

setting said DBW value to said LKDBW value when said LOCK signal is not asserted, and setting said DBW value to said TKDBW value when said LOCK signal is asserted.

19. The method of claim 18, further comprising:

programming said LKTBW value, said LKDBW value, said TKTBW value, and said TKDBW value into said first LK reloadable register portion, said second LK reloadable register portion, said first TK reloadable register portion, and said second TK reloadable register portion, respectively, by software from a computer system.

20. The method of claim 15, further comprising:

programming said TBW value and said DBW value into said first reloadable register portion and said second reloadable register portion, respectively, by software from a computer system.

21. The method of claim 15, wherein said phase transition detector, said digital filter, and said phase selector comprise said DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

22. A DPLL (digital phase locked loop) for generating a recovered clock signal, comprising:

a phase detector operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals;

a phase selector operable to select a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals in response to FWD (forward) and BWD (backward) signals; and

a digital filter coupled between the phase detector and the phase selector, the digital filter operable to generate the FWD and BWD signals for the phase selector in response to the up and down signals received from the phase detector;

wherein the digital filter includes at least one reloadable register operable to store a programmable value for comparison with a value derived from the up and down signals and a controller responsive to the comparison and operable to generate the FWD and BWD signals.

23. The DPLL (digital phase locked loop) of claim 22, wherein the DPLL (digital phase locked loop) is part of a clock data recovery circuit within a SERDES (serializer/deserializer) transceiver.

24. The DPLL (digital phase locked loop) of claim 22, wherein said phase selector includes a phase interpolator coupled to a multiplexer responsive to the FWD and BWD signals, the multiplexer operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as one of the given clock signals as outputs, the phase interpolator operable to generate the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

25. The DPLL (digital phase locked loop) of claim 22, wherein the digital filter includes:

at least two reloadable registers, each operable to store a programmable value;

a subtractor operable to generate a value representing a difference between counts of up and down signal pulses received from the phase detector;

an adder operable to generate a value representing a sum of counts of the up and down signal pulses;

a first comparator coupled to a first reloadable register and to the subtractor and operable to generate a signal based on comparison of the first register's programmable value and the difference value;

a second comparator coupled to a second reloadable register and to the adder and operable to generate a signal based on comparison of the second register's programmable value and the sum value; and

a controller responsive to the signals generated by the first and second comparators and operable to generate the FWD and BWD signals.

26. A digital filter comprising:

at least two reloadable registers, each operable to store a programmable value;

a subtractor operable to generate a value representing a difference between

counts of received up and down signal pulses;

an adder operable to generate a value representing a sum of counts of the received up and down signal pulses;

a first comparator coupled to a first reloadable register and to the subtractor and operable to generate a signal based on comparison of the first register's programmable value and the difference value;

a second comparator coupled to a second reloadable register and to the adder and operable to generate a signal based on comparison of the second register's programmable value and the sum value; and

a controller responsive to the signals generated by the first and second comparators and operable to generate FWD and BWD signals.

27. The digital filter of claim 26 including a first counter operable to count received up signal pulses and a second counter operable to count received down signal pulses.

28. A method for generating a recovered clock signal comprising:

comparing a serial data input (SDIN) with a recovered clock signal (SCLK) and generating in response up and down signals;

deriving a value from the up and down signals;

comparing a programmable value with the derived value;

generating FWD (forward) and BWD (backward) signals in response to the comparison of the programmable value and derived value; and

selecting a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals in response to the FWD and BWD signals.

29. The method of claim 28, wherein said step of selecting said recovered clock

signal (SCLK) includes the steps of:

selecting at least two clock signals from a plurality of given clock signals having different phases in response to the FWD and BWD signals; and

generating the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

30. The method of claim 28, wherein deriving a value from the up and down signals comprises generating a value representing a difference between counts of up and down signal pulses.

31. The method of claim 28, wherein deriving a value from the up and down signals comprises generating a value representing a sum of counts of up and down signal pulses.

32. A method for digitally filtering signals within a DPLL (digital phase locked loop) comprising:

generating a value representing a difference between counts of received up and down signal pulses;

generating a value representing a sum of counts of the received up and down signal pulses;

comparing the difference value to a first programmable value;

comparing the sum value to a second programmable value; and

generating FWD (forward) and BWD (backward) signals based on the comparisons.